WHAT IS CLAIMED IS:

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1. A multilayered wiring structure for high frequency semiconductor devices, comprising:

a semiconductor substrate;

a ground plate formed above said semiconductor substrate, having a potential fixed at the ground potential;

a plurality of wiring layers, each of which is alternately stacked with insulating interlayer formed above said semiconductor substrate, the wiring layers combining with said ground plate to form transmission lines; and

at least one separation electrode being selectively provided on the additional insulating interlayers, said at least one separation electrode having a potential fixed at the ground potential;

wherein said at least one separation electrode is formed near the crossing portion where the wiring layers mutually cross, with insulating interlayers provided therebetween.

2. A multilayered wiring structure for high frequency semiconductor devices, according to Claim 1, wherein the size of said at least one separation electrode is sufficiently smaller than the length of each of the transmission lines above said semiconductor substrate.

3. A multilayered wiring structure for high frequency semiconductor devices, according to Claim 1, wherein each of the crossing portions has the separation electrode.

4. A multilayered wiring structure for high frequency semiconductor devices, according to Claim 3, wherein the separation electrodes are electrically interconnected.

5. A multilayered wiring structure for high frequency semiconductor devices, according to Claim 3, wherein the separation electrodes have a potential which is fixed at the ground potential by a common electrode.

6. A multilayered wiring structure for high frequency semiconductor devices, according to Claim 4, wherein the separation electrodes are provided on one of the insulating interlayers, and are electrically interconnected by wiring extended on said insulating interlayer.

7. A multilayered wiring structure for high frequency semiconductor devices, according to Claim 4, wherein the separation electrodes are provided on different insulating interlayers, and are electrically interconnected by at least one throughhole.

8. A multilayered wiring structure for high frequency semiconductor devices, according to Claim 1, wherein a single separation electrode is in common provided for all of the crossing portions.

9. A multilayered wiring structure for high frequency semiconductor devices, according to Claim 3, wherein the crossing portions are positioned at different levels, and the separation electrodes are provided on those of the insulating interlayers which are provided in common in the crossing portions.

10. A multilayered wiring structure for high frequency semiconductor devices, according to Claim 8, wherein the crossing portions are positioned at different levels, and said single separation electrode is provided on one of the insulating interlayers which is provided in common in the crossing portions.